

# SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE $\bar{S}$ - $\bar{R}$ LATCHES

SDLS093 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

## description

The '279 offers 4 basic  $\bar{S}$ - $\bar{R}$  flip-flop latches in one 16-pin, 300-mil package. Under conventional operation, the  $\bar{S}$ - $\bar{R}$  inputs are normally held high. When the  $\bar{S}$  input is pulsed low, the Q output will be set high. When  $\bar{R}$  is pulsed low, the Q output will be reset low. Normally, the  $\bar{S}$ - $\bar{R}$  inputs should not be taken low simultaneously. The Q output will be unpredictable in this condition.

FUNCTION TABLE  
(each latch)

INPUTS		OUTPUT
$\bar{S}^\dagger$	$\bar{R}$	Q
H	H	$Q_0$
L	H	H
H	L	L
L	L	$H^\ddagger$

H = high level      L = low level

$^\dagger$ For latches with double S inputs:

$Q_0$  = the level of Q before the indicated input conditions were established.

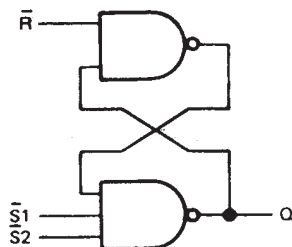
$^\ddagger$  This configuration is nonstable; that is, it may not persist when the  $\bar{S}$  and  $\bar{R}$  inputs return to their inactive (high) level.

H = both  $\bar{S}$  inputs high

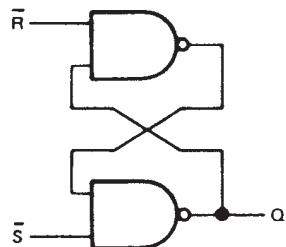
L = one or both  $\bar{S}$  inputs low

## logic diagram (positive logic)

(latches 1 and 3)



(latches 2 and 4)

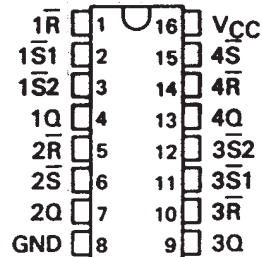


SN54279, SN54LS279A . . . J OR W PACKAGE

SN74279 . . . N PACKAGE

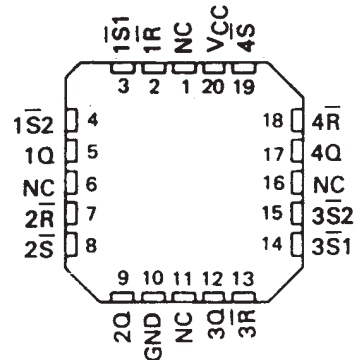
SN74LS279A . . . D OR N PACKAGE

(TOP VIEW)



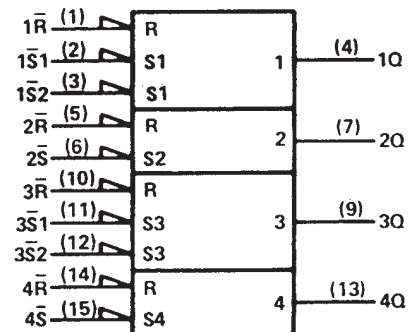
SN54LS279A . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

## logic symbol<sup>§</sup>



<sup>§</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

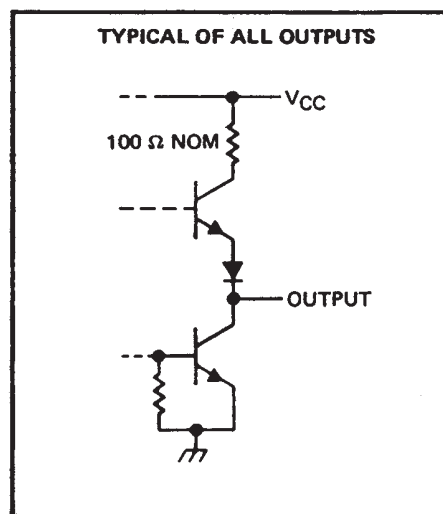
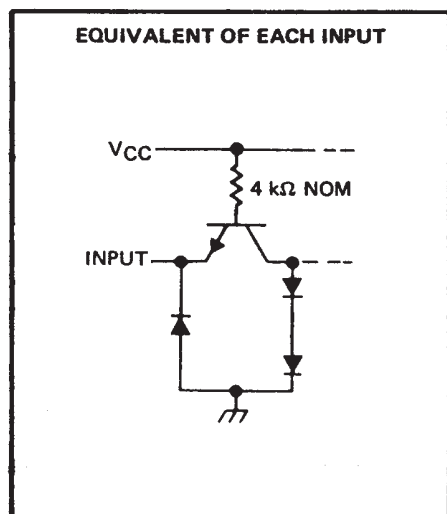
Pin numbers shown are for D, J, N, and W packages.

# SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

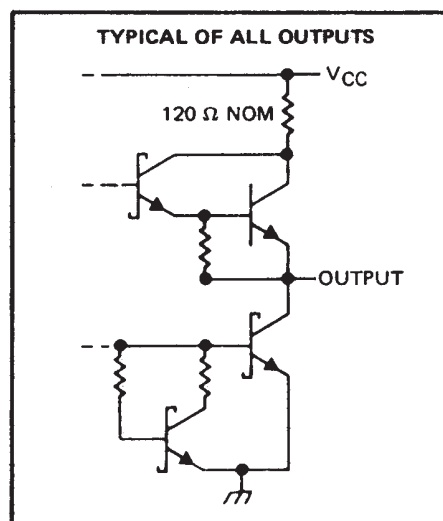
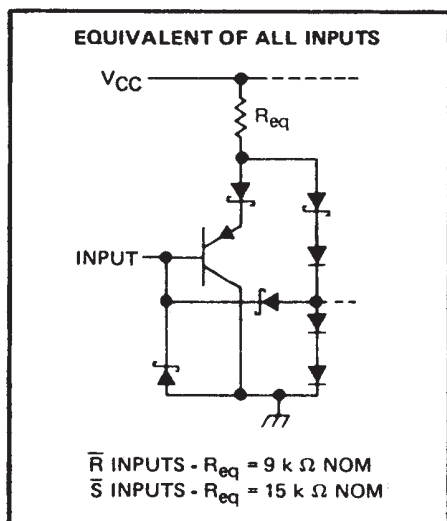
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## schematics of inputs and outputs

### '279 CIRCUITS



### 'LS279A CIRCUITS



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '279	5.5 V
'LS279A	7 V
Operating free-air temperature range: SN54' TYPES	– 55° C to 125° C
SN74' TYPES	0° C to 70° C
Storage temperature range	– 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

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## recommended operating conditions

	SN54279			SN74279			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.8			0.8	V
I <sub>OH</sub> High-level output current			– 0.8			– 0.8	mA
I <sub>OL</sub> Low-level output current			16			16	mA
t <sub>w</sub> Pulse duration, low	20			20			ns
T <sub>A</sub> Operating free-air temperature	– 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54279			SN74279			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = – 12 mA			– 1.5			– 1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = – 0.8 mA	2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40			40	µA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			– 1.6			– 1.6	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	– 18		– 55	– 18		– 57	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2		18	30		18	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I<sub>CC</sub> is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	$\bar{S}$	Q	R <sub>L</sub> = 400 Ω, C <sub>L</sub> = 15 pF		12	22	ns
t <sub>PHL</sub>	$\bar{R}$	Q			9	15	
t <sub>PHL</sub>	$\bar{R}$	Q			15	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

# SN54279, SN54LS279A, SN74279, SN74LS279A QUADRUPLE S-R LATCHES

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## recommended operating conditions

	SN54LS279A			SN74LS279A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
I <sub>OH</sub> High-level output current			– 0.4			– 0.4	mA
I <sub>OL</sub> Low-level output current			4			8	mA
t <sub>w</sub> Pulse duration, low	20			20			ns
T <sub>A</sub> Operating free-air temperature	– 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS279A			SN74LS279A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = – 18 mA			– 1.5			– 1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, I <sub>OH</sub> = – 0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4	V
	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA					0.25	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			– 0.2			– 0.2	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	– 20		– 100	– 20		– 100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See note 2		3.8	7		3.8	7	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should be less than one second.

NOTE 2: I<sub>CC</sub> is measured with all R inputs grounded, all S inputs at 4.5 V, and all outputs open.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	$\bar{S}$	Q	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		12	22	ns
t <sub>PHL</sub>					13	21	
t <sub>PHL</sub>	$\bar{R}$	Q			15	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
76018012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
7601801EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7601801EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7601801FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7601801FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54279J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54279J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS279AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS279AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74279N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74279N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74279N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74279N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS279AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS279AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS279AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS279AN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS279ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS279ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS279ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS279ANSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54279J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54279J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54279W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54279W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS279AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS279AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS279AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS279AJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS279AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS279AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS279ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS279ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS279ADR	SOIC	D	16	2500	342.9	345.9	28.6
SN74LS279ANSR	SO	NS	16	2000	346.0	346.0	33.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.  
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.  
E. Reference JEDEC MS-012 variation AC.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.